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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/002,217	Applicant(s) NEMECEK, CRAIG	
	Examiner Jason Proctor	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action of 3 April 2006.

Applicants' response of 10 July 2006 submits claims 1-20 for reconsideration.

Claims 1-20 are rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is <u>denied</u>, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Claim Interpretation

2. The Examiner thanks Applicants for clarification regarding the intended interpretation of the claim language. Specifically, Applicants submit that:

> Claim 1 specifically invokes 35 U.S.C. § 112, sixth paragraph, and should be interpreted in light of the entire specification and equivalent thereof <u>and not</u> in light of other claims as suggested by the rejection.

The Examiner has fully considered this argument and finds it fully persuasive.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 6, 9-12, 14, and 17-20 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 6 (and similarly claim 14) define a method that does not produce a useful, concrete, and tangible result. These methods define steps of detecting, computing a conditional jump address, and determining … whether to proceed. Such a determination is not a useful, concrete, and tangible result.

In contrast, claims 7 and 8 (15 and 16) positively recite executing an instruction based upon the determination. These claims establish a useful, concrete, and tangible result for the methods of the parent claim.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

4. Claim 13 is rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 13 defines descriptive material and is therefore non-statutory. As an apparatus claim, this would be statutory according to MPEP 2106. However, claim 13 depends from "the

method according to claim 6," and therefore cannot be properly interpreted as an apparatus claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 13 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13, as written, depends from the *method* of claim 6 but fails to further define that method. Further, the claim language defines a *separate and distinct* invention from the parent claim 6. A "method ... stored as instructions stored in an electronic storage medium" defines non-statutory data and does not further define a method.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-4, 6-11, and 13-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,366,878 to Grunert in view of "Structured Computer Organization, Fourth Edition" by Andrew S. Tanenbaum with contributions by James R. Goodman (hereafter referred to as Tanenbaum).

Regarding claim 1, Grunert teaches:

An In-Circuit Emulation system [*"a circuit arrangement for in-circuit emulation"* (column 1, lines 66-67)], comprising:

A microcontroller [*"comprising a first ... microcontroller"* (column 1, line 66 – column 2, line 1)] having a microcontroller clock [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)]; and

A virtual microcontroller [*"comprising ... a second microcontroller"* (column 1, line 66 – column 2, line 1)] coupled to and executing instructions in lock-step with the microcontroller [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)] by executing the same instructions [*"The microcontrollers have an ROM memory 8, 8' in which the operating program is otherwise stored in normal operation. During in-circuit emulation, the memory 8, 8' is switch off... The master 2 is connected to the external memory 4 by means of its ports P0, P2... The data D read out from the memory 4 are also fed to the slave 3."* (column 4, lines 29-53); That is, during in-circuit emulation, both microcontrollers (2, 3) receive the same operating program from external

memory 4, thus execute the same instructions.] using the same clocking signals [*"A clock system 5 ensures good synchronization between master 2 and slave 3."* (column 5, lines 8-9); *"a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)] and wherein the microcontroller sends I/O read data to the virtual microcontroller [*"The master 2 processes the operating program by evaluating the data, input externally via the ports P0, ..., P4, from the application system. Feeding the operating program to the slave 3 serves the purpose of properly timing the control of the data input and output via the ports P0', P2', P3'."* (column 4, line 67 – column 5, line5); I/O read data present in the operating program and evaluated by the master 2 is sent to the virtual microcontroller to also evaluate the same I/O read data].

Grunert does not expressly disclose the limitations regarding "means for detecting an I/O read instruction followed (immediately) by a conditional jump instruction, and for computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller, and further having means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution at a next consecutive address or at the conditional jump address."

Tanenbaum teaches "Branch Prediction," (page 270, § 4.5.2). Tanenbaum teaches branch prediction for conditional branches [*"Consequently, what most machines do when they hit a conditional branch is predict whether it is going to be taken or not."* (page 272)]. Tanenbaum teaches "computing a conditional jump address prior (to execution of the jump instruction) [*"If a*

branch is correctly predicted, there is nothing special to do. Execution just continues at the target address." (page 272); Here Tanenbaum clearly teaches that "execution just continues" because the target address of the branch instruction is already known, i.e. precomputed].

Tanenbaum expressly teaches motivation for implementing branch prediction [*"All computer manufacturers want their systems to run as fast as possible... Consequently, most of the ideas we will discuss are already in use in a wide variety of existing products."* (page 264); *"Early pipelined machines just* ***stalled*** *until it was known whether the branch would be taken or not. Stalling for three or four cycles on every conditional branch, especially if 20% of the instructions are conditional branches, wreaks havoc with performance."* (page 272); *"Clearly, having the predictions be accurate is of great value, since it allows the CPU to proceed at full speed."* (page 273)].

Tanenbaum and Grunert are both directed to processor architecture and are therefore analogous prior art.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that I/O instructions are slow instructions that generally take "three or four cycles" or even longer. It would therefore be obvious to a person of ordinary skill in the art at the time of Applicants' invention, because of the teachings of Tanenbaum, that the performance of a processor, in the case of Grunert a microcontroller, can be improved by using branch prediction where a branch instruction depends on the result of an I/O instruction. In addition to being "already in use in a wide variety of existing products," such an improvement would help the system to "run as fast as possible."

Therefore, upon identifying the synchronization problem where the virtual microcontroller executes an I/O read instruction immediately followed by a conditional branch (jump) instruction, it would have been obvious to a person of ordinary skill in the art to combine Tanenbaum's teaching of branch prediction to "compute a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller," thus helping the system to "run as fast as possible." As taught by Tanenbaum, branch prediction requires "means for determining whether to proceed with instruction execution at a next consecutive address or at the conditional jump address" (as cited above and exemplified on page 271).

Claim 2 recites an implicit limitation of claim 1. "Wherein the conditional jump address is computed while the I/O read data are sent from the microcontroller to the virtual microcontroller" is regarded as functionally equivalent to "computing a conditional jump address prior to receipt of I/O read data from the microcontroller" and "wherein the microcontroller sends I/O read data to the virtual microcontroller."

Regarding claims 3 and 4, Tanenbaum teaches an instruction wherein the processor sets a zero flag if an I/O read test condition is met [*"The next two groups deal with testing and comparing, and then jumping based on the results. The results of test and compare instructions are stored in various bits of the EFLAGS register. Jxx stands for a set of instructions that conditionally jump, depending on the results of the previous comparison (i.e., the bits in EFLAGS)."* (page 360)]. The limitation "wherein the jump conditions is met if the zero flag is

set" is taught by Tanenbaum (page 360) especially when read by one of ordinary skill in the art. This claim describes a "jump if zero" or JZ assembly instruction.

Claim 6 recites a method performed by the system of claim 1. Claim 6 is therefore rejected for rationale similar to that given above regarding claim 1.

Claims 7 and 8 recite limitations implicit in claim 6. Claims 7 and 8 recite "executing a next consecutive instruction" and "executing an instruction at the conditional jump address" based on whether the conditional jump condition is met, as appropriate. These limitations are implicit from claim 6, reciting "a method of handling conditional jumps in the virtual microcontroller." Failure to perform the steps of claims 7 and 8 would render the system of claim 6 inoperative. Therefore, claims 7 and 8 are rejected for rationale similar to that given above regarding claim 6.

Claim 9 recites limitations that correspond to claim 2. Claim 9 is therefore rejected for rationale similar to that given above regarding claim 2.

Claims 10 and 11 recite limitations that correspond to claims 3 and 4. Claims 10 and 11 are therefore rejected for rationale similar to that given above regarding claims 3 and 4.

Regarding claim 13, Tanenbaum teaches that the method is stored as instructions for execution by a programmed processor [*"A different way to go is to have the compiler help out."* (page 275)].

Claim 14 recites a method corresponding to claim 6 wherein "microcontroller" is replaced by "device under test." As a microcontroller in the claimed system constitutes a "device under test," claim 14 is rejected for rationale similar to that given above regarding claim 6.

Claims 15-19 recite limitations that correspond to claims 7-11. Claims 15-19 are therefore rejected for rationale similar to that given above regarding claims 7-11.

In response to the previous rejections of claims 1-4, 6-11, and 13-19 as unpatentable over Grunert in view of Tanenbaum, Applicants argue primarily that:

> Grunert fails to disclose or suggest that the microcontroller sends I/O read data to the virtual microcontroller, as claimed but instead discloses that the external memory component sends data byte read out to both master and the slave microcontrollers.

The Examiner respectfully traverses this argument as follows.

To quote Applicants' argument, "Grunert discloses that the master microcontroller feeds the <u>memory address</u> to the external memory component (see Grunert, col. 4, lines 41-44). Data byte from the external memory component is then read out and fed to the master microcontroller and the slave microcontroller (see Grunert, col. 4, lines 47-53)." There appears to be agreement that the master microcontroller initiates a process (feeds a memory address to the external memory component) which results in external data being fed to the virtual microcontroller (slave

microcontroller). It cannot be said that the slave microcontroller obtains this external data of its own volition. Only when the master microcontroller initiates this specific process is external data fed to the slave microcontroller. Therefore the master microcontroller sends I/O read data to the virtual microcontroller. There claim language does not appear to exclude this system taught by Grunert.

Further, the claim specifies that the microcontroller and the virtual microcontroller operate in lock-step "by executing the <u>same instructions</u> using the same clocking signals." The system taught by Grunert teaches the claim because the microcontroller "sends I/O read data to the virtual microcontroller" as explained above, yet the two execute the <u>same instructions</u>, as claimed.

Applicants further argue that:

> The rejection inappropriately presume that based on this disclosure, execution of the <u>same</u> instruction <u>using</u> the same clocking signal, as claimed follows. The Applicant respectfully disagrees because the mere fact that the data D read out is fed to both master and slave and that good synchronization between master and slave exists <u>does not necessarily</u> translate to execution of the same instructions using the same clocking signals, as claimed.

The Examiner respectfully traverses this argument as follows.

Applicants' allegation that Grunert's master microcontroller and slave microcontroller, which art taught as "identical microcontrollers" (column 1, line 66 – column 2, line 26), which execute the same instructions (column 4, line 66 – column 5, line 5), and are clocked by the same clock source (column 5, lines 8-9; FIG. 1, reference 5) "does not necessarily translate to execution of the same instructions using the same clocking signals" is not clearly understood. Applicants continue:

> For example, the data D read out may be fed to both master and slave with good synchronization between the two microcontrollers, however processing of data D read out by the slave may be significantly after processing of data D read out by the master. Grunert fails to explicitly disclose or suggest virtual microcontroller and the microcontroller executing the same instruction using the same clocking signal, as claimed.

It is unclear where support for this conclusion is found in the reference. The Examiner understands Grunert as explicitly teaching the opposite of Applicants' conclusion. That is, Grunert explicitly teaches processing of data D by the master and slave microcontroller in synchronization (column 4, line 40 – column 5, line 8) using the same clocking signal (column 5, lines 3-8; FIG. 1, reference 5).

Applicants further argue that:

> In fact, Grunert teaches away from execution of the same instruction using the same clocking signals, as claimed. Grunert discloses that the slave microcontroller ports P0', P2', and P3' serve as external connections of the overall circuit arrangement (see Grunert, col. 4, lines 59-61) and that feeding the operating program to the slave microcontroller serves the purpose of properly timing the control of the data input and output via the ports P0', P2' and p3' (see Grunert, col. 5, lines 3-5). Therefore, feeding the operating program to the slave microcontroller provides proper timing with external connections of the overall circuit arrangement and not with the master microcontroller (see Grunert, Figure 1). As such, Grunert teaches away because the purpose of feeding the operating program to the slave microcontroller is not execution of the same instructions using the same clocking signals by the virtual microcontroller and the microcontroller, as claimed but is instead to provide proper timing between the slave microcontroller and external connections of the overall circuit arrangement.

The Examiner respectfully traverses this argument as follows.

The Examiner has fully considered Applicants' argument and the portions of Grunert cited therein. However, none of this establishes that Grunert teaches that "execution of the same instructions using the same clocking signals" is somehow inferior, undesirable, or unsuitable. Therefore, Grunert does not "teach away" from the limitation as alleged by Applicants.

Applicants further argue that:

> Tanenbaum discloses that what most machines do <u>when they hit a conditional branch</u> is to predict whether it is going to be taken or not and if a branch is correctly predicted execution continues at the target address (see Tanenbaum, page 272). Accordingly Tanenbaum discloses predicting whether to take a conditional branch <u>when a conditional branch</u> is hit and not computing a conditional jump address <u>prior</u> to receipt of I/O read data from the microcontroller, as claimed.

The Examiner respectfully traverses this argument as follows.

Microsoft Computer Dictionary, Fifth Edition, defines:

> **branch prediction** *n.* A technique used in some processors with an instruction called prefetch to guess whether or not a branch will be taken in a program, and to fetch executable code from the appropriate location. When a branch instruction is executed, it and the next instruction executed are stored in a buffer. This information is used to predict with way the instruction will branch the next time it is executed. When the predictions is correct (as it is over 90 percent of the time), executing a branch does not cause a pipeline break, so the system is not slowed down by the need to retrieve the next instruction.

Applicants' argument appears to force the Tanenbaum reference into the awkward position of contradicting the industry standard terminology as used and known in the art. This argument is unpersuasive.

Applicants further argue that:

> Moreover, the rejection does not address the limitation whereby the virtual microcontroller having means for detecting an I/O read instruction followed by a conditional jump instruction to remain in lockstep execution with the microcontroller, as claimed. Moreover, the Applicant does not understand Tanenbaum to disclose or suggest the recited limitation.

The Examiner respectfully traverses this argument as follows.

The Examiner respectfully submits that a microcontroller executing an I/O read instruction followed by a conditional jump instruction, as taught by Grunert, satisfies the claimed

"means for detecting an I/O read instruction followed by a conditional jump instruction." Secondly, Tanenbaum teaches a means for keeping two microcontrollers in lockstep, as claimed, specifically "branch prediction". Lastly, the claim does not recite the phrase as presented in Applicants' argument.

7. Claims 5, 12, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Grunert in view of Tanenbaum as applied to claims 1 and 6 above, and further in view of US Patent No. 6,173,419 to Barnett.

Neither Grunert nor Tanenbaum expressly teach that the virtual microcontroller is implemented in a field programmable gate array (FPGA).

Barnett teaches the use of an FPGA as a hardware emulator (abstract; column 2, lines 11-16; column 5, lines 38-56). Barnett teaches that the advantage of such an arrangement is the reuse of the hardware emulator for different configurations (column 2, lines 41-51).

Barnett, Tanenbaum, and Grunert are all directed to processor architecture and are therefore analogous prior art.

Therefore, it would have been obvious for a person of ordinary skill in the art at the time of Applicants' invention to implement the slave microcontroller taught by Grunert in an FPGA, according to the method taught by Barnett, in order to provide an in-circuit emulator system that facilitates emulating the emulated microcontroller in different configurations of target circuitry. Barnett expressly provides motivation for doing so [*"What is needed is an emulator for debugging software that operates in real time, is economical to create, and may be programmed*

to have a variety of configurations." (column 2, lines 6-9)]. The combination could be achieved by implementing the slave microcontroller taught by Grunert as emulated by an FPGA connected to and configured by the host computer.

Regarding the rejections of claims 5, 12, and 20, Applicants refer to the alleged deficiencies of the Grunert and Tanenbaum references which have been addressed above.

8. Claims 1, 3-5, 6-8, 10-13, 14-16, and 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,016,563 to Fleischer in view of US Patent No. 6,366,878 to Grunert and further in view of "Evaluation of a Branch Target Address Cache" by Sreeram Duvvuru and Siamak Arya (hereafter referred to as Duvvuru).

Regarding claim 1, Fleischer teaches an in-circuit emulation system (abstract) comprising

A programmable device [*"development, verification, and testing, in a real-time user target environment, of complex programmable logic devices, such as electrically programmable logic devices (EPLDs), field-programmable gate arrays (FPGAs), programmable array logic (PAL) devices, application-specific integrated circuits (ASICs), etc."* (column 2, lines 46-60)];

A second programmable device coupled to and executing instructions in lock-step with the first programmable device by executing the same instructions using the same clocking signals [*"Generally, an emulation system of the present invention includes a symmetrical pair of programmable logic devices, i.e., the target programmable logic device and a programmable logic device that is essentially identical to the target device and is referred to herein as the*

"mirror" device or the "emulation" device." (column 2, line 61 – column 3, line 2); *"The mirror device ... operates as an exact replica of the target device in the user-defined target environment."* (column 2, line 66 – column 3, line 2)],

Wherein the first programmable device sends I/O read data to the second programmable device [*"The system 1 also includes a switching module 11 containing a number of individually programmable "zero ohm" switches SW1, SW2, and SW3, connected between the input/output (I/O) pins of the target device and the mirror device 10."* (column 3, lines 7-12); FIG. 4, references 15A, 15B, 16A, 16B, 17A, 17B, 18, etc.)]; and

The second programmable device has a means for detecting an I/O read instruction followed by a conditional jump instruction [inherent by virtue of executing those instructions].

Fleischer does not expressly teach that the programmable devices are microcontrollers.

Grunert teaches a system for in-circuit emulation of a microcontroller (title, abstract).

Neither Grunert nor Fleischer expressly teach a virtual microcontroller with means of computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller; and the virtual microcontroller further having means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution at a next consecutive address or at the conditional jump address.

Duvvuru teaches means of computing a conditional jump address prior to receipt of I/O read data [*"Our scheme relies on the fact that the condition code upon which a branch is based can be determined slightly ahead of the branch."* (page 174, right column); *"Register Relative branch instruction is emitted to implement a branch where the target is dynamically set. The branch target address is either computed on the fly or* ***loaded from memory****."* (page 176, right column, emphasis added); *"Register-relative branches may be cacheable, provided the compiler or linker can guarantee that the target address does not change."* (page 176, right column – page 177, left column)]; and

Means for determining after receipt of the I/O read data whether to proceed with instruction execution at a next consecutive address or at the conditional jump address [*"If we hit in the BTAC the target address and associated cc bit number are read out. If the specified cc bit is set in the CCR, the next-pc is set to the cached target address, otherwise it is set to the start of the next sequential issue group."* (page 174, right column)].

Duvvuru, Grunert, and Fleischer are all analogous art because all are directed to processor architecture.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the microcontrollers taught by Grunert with the emulation system of Fleischer, using microcontrollers as the first and second programmable devices. Motivation is found in Grunert, such as modifying the operating program within a microcontroller during an emulation phase [*"In particular, there is a need to provide a*

possibility of access to the operating program of the microcontroller, which in normal operation is stored in an ROM memory which is not directly accessible from outside. The operating program can thereby be changed during the development phase." (column 1, lines 9-22)].

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the branch prediction taught by Duvvuru with the combination of Grunert in view of Fleischer to utilize branch prediction during execution of instruction code on the microcontrollers. Motivation is found in Duvvuru, such as improving the execution performance of the processors [*"Two key issues need to be resolved to alleviate this problem: a branch resolution scheme... and mechanisms to minimize the impact of unpredictable branches. We propose a technique of cacheing branch target addresses... that would allow the bgranch decision to be made in the fetch stage of the pipeline... Impact of register-relative branches which may have variable target addresses is considered and a solution is suggested."* (page 173, left column, abstract)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Duvvuru, Grunert, and Fleischer in order to arrive at the invention as specified in claim 1.

Regarding claim 5, Fleischer teaches implementing the virtual microcontroller in a Field Programmable Gate Array (column 2, lines 46-60).

Claims 6-8 and 10-12 recite a method employed by the system of claims 1 and 3-5. As Fleischer in view of Grunert and further in view of Duvvuru renders the system of claims 1 and 3-5 obvious, claims 6-8 and 10-12 are rendered obvious for similar rationale.

Claim 13 defines stored computer software. Fleischer teaches computer software (column 6, lines 46-56).

Claims 14-16 and 18-20 define a broader recitation of the system of claims 6-8 and 10-12, and are rendered obvious over Fleischer in view of Grunert and further in view of Duvvuru for rationale similar to that explained above.

9. Claims 3 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fleischer in view of Grunert in view of Duvvuru as applied to claim 1 above, and further in view of Official Notice.

Claims 3 and 4 define what is known in the art as a "Jump if zero" conditional branch instruction. Official notice is taken that a "jump if zero" instruction is well known in the art, that such an instruction "sets a zero flag" if a condition is met, and the "jump condition is met if the zero flag is set."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

9/28/06